IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:		§		
	Dennis M. O'Connor	§	Art Unit:	2186
		§		
Serial No.:	10/773,847	§		
		§	Examiner:	Pierre Miche Bataille
Filed:	February 5, 2004	§		
		§		
For:	Address Conversion Technique in a Context Switching Environment	§	Docket:	ITL.1806US P15392

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-24 (Rejected).

Claims 1-24 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

No amendments were made in the Reply to Final Rejection submitted on September 22, 2008. All amendments have therefore been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims.

Embodiments of the present invention relate to a memory management unit (Fig. 2). The memory management unit stores generated virtual address-to-physical address translations. If a virtual address-to-physical address translation is available for a particular virtual address, the memory management unit retrieves the corresponding physical address. If a translation is not available, the memory management unit generates the corresponding physical address from the virtual address. The memory management unit converts the virtual address to a modified virtual address using a process identifier and then performs a page table walk using the modified virtual address, generating the physical address. (Paragraph [1009])

Referring to Appellant's independent claim 1, by way of example, a memory management unit is claimed. (Fig. 2; paragraph [1018]) The memory management unit is configured to receive a virtual address and provide a corresponding physical address. (Fig. 2; paragraph [1018]) The memory management unit includes a storage containing one or more virtual address-to-physical address translations. (Fig. 2, 202; paragraph [1018]) The memory management unit also includes conversion logic to generate a modified virtual address from the virtual address if a virtual address-to-physical address translation for the virtual address does not exist in the storage. (Fig. 2, 206; paragraph [1018]) The memory management unit also includes a page table walk unit configured to convert the modified virtual address into the corresponding physical address. (Fig. 2, 208; paragraph [1020])

Referring to independent claim 11, by way of example, a system is claimed. (Fig. 1; paragraph [l015]) The system includes an antenna (Fig. 1, 108; paragraph [l017]), a memory (Fig. 1, 106; paragraph [1016]), and a processor coupled to the antenna and memory (Fig. 1, 100; paragraph [1016]). The processor includes an address generation unit (Fig. 1, 102; paragraph [1015]) and a memory management unit (Fig. 1, 104; paragraph [1015]). The memory management unit is configured to receive a virtual address from the address generation unit and provide a corresponding physical address (Fig. 2; paragraph [1018]). The memory management unit includes a storage containing one or more virtual address-to-physical address translations (Fig. 2, 202; paragraph [1018]); conversion logic to generate a modified virtual address from the

virtual address if a virtual address-to-physical address translation for the virtual address does not exist in the storage (Fig. 2, 206; paragraph [1018]); and a page table walk unit configured to convert the modified virtual address into the corresponding physical address (Fig. 2, 208; paragraph [1020]).

Referring to independent claim 17, by way of example, a method is claimed. The method includes receiving a virtual address at a memory management unit (Fig. 2; paragraph [1018]); determining if the virtual address has a translation to a physical address in a storage (Fig. 2, 202; paragraph [1018]); if not, generating a modified virtual address from the virtual address (Fig. 2, 206; paragraph [1018]); and translating the modified virtual address into a physical address (Fig. 2, 208; paragraph [1020]).

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1-24 are anticipated under 35 U.S.C. § 102(b) by Chauvel (US 2002/062434).

ARGUMENT

A. Are claims 1-24 are anticipated under 35 U.S.C. § 102(b) by Chauvel (US 2002/062434)?

The brief summary of the invention summarizes what is set forth in greater detail in paragraphs 39-45. In the event of a miss, the TLB control 70 provides a signal that there is no match in the TLB memory 72. See paragraph 39. There are two approaches to this problem. In the first approach, a hardware approach, described in paragraph 41, "The virtual address, resource identifier and task identifier are presented to a logical circuit." See paragraph 41.

There is no conversion logic to generate a modified virtual address from the virtual address if a virtual address to physical address translation for the virtual address does not exist in the storage. Instead, the virtual address itself is utilized, not a modified virtual address. Moreover, the claim requires a page table walk unit configured to convert the modified virtual address into the corresponding physical address. This, too, cannot exist in the cited reference because there never is a modified virtual address.

The software embodiment, described in paragraph 45, operates similarly.

Thus, neither embodiment in any way supplements the deficiencies of the embodiment of the background of the invention described in paragraphs 7 and 8. Therefore, a *prima facie* rejection is not made out and reconsideration would be appropriate.

* * *

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: December 4, 2008

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CLAIMS APPENDIX

The claims on appeal are:

1. A memory management unit configured to receive a virtual address and provide a corresponding physical address, the memory management unit comprising:

a storage containing one or more virtual address-to-physical address translations;

conversion logic to generate a modified virtual address from the virtual address if a virtual address-to-physical address translation for the virtual address does not exist in the storage; and

a page table walk unit configured to convert the modified virtual address into the corresponding physical address.

2. The memory management unit as recited in Claim 1, wherein the conversion logic is configured to replace one or more bits of the virtual address with a process identifier if the one or more bits comprises a predetermined value.

3. The memory management unit as recited in Claim 2, wherein the predetermined value is zero.

4. The memory management unit as recited in Claim 1, wherein the memory management unit is configured to receive the virtual address from an arithmetic logic unit.

5. The memory management unit as recited in Claim 1, wherein the memory management unit is configured to receive the virtual address from an incrementor.

6. The memory management unit as recited in Claim 1, wherein the virtual address comprises a data address.

7. The memory management unit as recited in Claim 1, wherein the virtual address comprises an instruction address.

8. The memory management unit as recited in Claim 1, wherein the one or more virtual address-to-physical address translations are invalidated upon updates to a process identifier.

9. The memory management unit as recited in Claim 1, wherein only virtual address-to-physical address translations having a virtual address portion with one or more bits equal to a predetermined value are invalidated upon updates to a process identifier.

10. The memory management unit as recited in Claim 1, wherein the storage is configured to store one or more most recently generated virtual address-to-physical address translations.

11. A system comprising:

an antenna;

a memory; and

a processor coupled to the antenna and memory, the processor comprising:

an address generation unit; and

a memory management unit configured to receive a virtual address from the address generation unit and provide a corresponding physical address, the memory management unit comprising:

a storage containing one or more virtual address-to-physical address translations;

conversion logic to generate a modified virtual address from the virtual address if a virtual address-to-physical address translation for the virtual address does not exist in the storage; and

a page table walk unit configured to convert the modified virtual address into the corresponding physical address.

12. The system as recited in Claim 11, wherein the conversion logic is configured to replace one or more bits of the virtual address with a process identifier if the one or more bits are equal to a predetermined value.

13. The system as recited in Claim 11, wherein the address generation unit comprises an arithmetic logic unit.

14. The system as recited in Claim 11, wherein the address generation unit comprises an incrementor.

15. The system as recited in Claim 11, wherein the one or more virtual address-to-physical address translations are invalidated upon updates to a process identifier.

16. The system as recited in Claim 11, wherein only virtual address-to- physical address translations having a virtual address portion with one or more bits equal to a predetermined value are invalidated upon updates to a process identifier.

17. A method comprising:

receiving a virtual address at a memory management unit;

determining if the virtual address has a translation to a physical address in a storage;

if not, generating a modified virtual address from the virtual address; and

translating the modified virtual address into a physical address.

18. The method as recited in Claim 17, wherein generating the modified virtual address comprises replacing one or more bits of the virtual address with a process identifier if the one or more bits are equal to a predetermined value.

19. The method as recited in Claim 17, wherein translating the modified virtual address comprises performing a page table walk.

20. The method as recited in Claim 17, further comprising invalidating all translations in the storage if a process identifier changes.

21. The method as recited in Claim 17, further comprising invalidating only translations in the storage having a virtual address portion that has one or more bits equal to a predetermined value.

22. The method as recited in Claim 17, further comprising placing any generated translations into the storage.

23. The method as recited in Claim 17, wherein the virtual address is a data address.

24. The method as recited in Claim 17, wherein the virtual address is an instruction address.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.